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Application Serial No: 10/521,908
Responsive to the Office Action mailed on: February 8, 2007

REMARKS

This Amendment is in response to the Office Action mailed on February 8, 2007. Claim 1 is amended editorially and is supported, for example, in the specification at page 7, lines 19-23 and page 8, lines 4-7 and in Figures 2 and 3. Claims 6-20 are cancelled without prejudice or disclaimer. Claims 21-25 are new. Claim 21 is new and is supported, for example, in the specification on page 11, line 14-page 12, line 7 and Figures 7A-7C. Claim 22 is new and is supported, for example, in the specification on page 12, lines 8-26 and Figures 8A-8C. Claim 23 is new and is supported, for example, in the specification on page 12, line 27-page 13, line 13 and Figures 9A-9C. Claim 24 is new and is supported, for example, in the specification on page 12, line 27-page 13, line 13 and Figures 10A-10C. Claim 25 is new and is supported, for example, in the specification on page 12, line 27-page 13, line 13 and Figures 11A-11C. No new matter is added. Claims 1-5 and 21-25 are pending.

§102 Rejections:

Claims 1-4 and 6 are rejected as being anticipated by Takakusa (JP Patent Application No. 5-225892). This rejection is traversed.

Claim 1 is directed to a chip resistor that requires, among other features, a resistive element including a flat surface, an insulation layer having a first surface in contact with the flat surface and a second surface opposite to the first surface and a plurality of electrodes provided on the flat surface. Claim 1 further requires that the electrodes are formed with a solder layer and that the solder layer extends beyond a respective one of the electrodes into contact with the second surface.

Takakusa does not disclose or suggest these features. Takakusa is directed to a chip type overcurrent protection element that includes electrodes (2a, 2b). However, nowhere does Takakusa disclose or suggest the use of a solder layer on each of the electrodes (2a, 2b). For at least these reasons claim 1 is not suggested by Takakusa and should be allowed. Claims 2-4 depend from claim 1 and should be allowed for at least the same reasons.

Claims 1 and 6 are rejected as being anticipated by Katsuno (US Patent No. 5,548,269). This rejection is traversed.

Katsuno does not disclose or suggest these features. Katsuno is directed to a chip resistor that includes electrodes (4a, 4b). However, nowhere does Katsuno disclose or suggest the use of a solder layer on each of the electrodes (4a, 4b). For at least these reasons claim 1 is not suggested by Katsuno and should be allowed.

Claims 1 and 3-6 are rejected as being anticipated by Nakamura (JP Patent Application No. 2002-184601). This rejection is traversed.

Nakamura does not disclose or suggest these features. Nakamura is directed to a chip resistor that includes electrodes (121, 122) and solder layers (131, 132). However, nowhere does Nakamura disclose or suggest that the solder layer (131, 132) extends beyond a respective one of the electrodes (121, 122) into contact with the second surface as required by claim 1. For at least these reasons claim 1 is not suggested by Nakamura and should be allowed. Claims 2-5 depend from claim 1 and should be allowed for at least the same reasons.

Conclusion:

Applicant respectfully asserts that claims 1-5 and 21-25 are now in condition for allowance. If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Applicant's primary attorney-of record, Douglas P. Mueller (Reg. No. 30,300), at (612) 455-3804.

Respectfully submitted,

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